What is claimed is:

1. A method of overerase correction for memory cells in a memory array after the memory cells have been erased, comprising the following steps:

(a) setting a gate voltage of memory cells from a first selected bit line exhibiting leakage current above a threshold value to an initial voltage level;

(b) applying a series of overerase correction pulses to said first selected bit line during a selected time period;

(c) detecting during said selected time period whether said bit line exhibits leakage current above said threshold value;

(d) if said bit line exhibits leakage current above said threshold value after said selected time period, increasing said gate voltage and repeating steps (b) and (c); and

(e) if it is detected that said bit line does not exhibit leakage current above said threshold value during said selected time period, selecting a second bit line and repeating steps (a) through (d).

2. The method of claim 1, wherein said selected time period is between about 20-100 milliseconds.

3. The method of claim 1, wherein each overerase correction pulse from said series of overerase correction pulses is applied for between about 0.5-2.0 milliseconds.

4. The method of claim 1, wherein step (c) comprises the following step:

detecting after each overerase correction pulse whether said bit line exhibits leakage current above said threshold value.

5. The method of claim 1, further comprising the step of setting an error flag if said gate voltage has reached a maximum gate voltage value.

6. The method of claim 1, wherein said initial voltage level is a negative voltage.

7. The method of claim 6, wherein said initial voltage level is approximately -2.0 V and step (d) includes the step of positively incrementing said gate voltage in increments of about 0.5 V.

8. A semiconductor device comprising a memory array including a plurality of memory cells disposed in a plurality of bit lines, said semiconductor device comprising circuitry for overerase correction of said memory cells after the memory cells have been erased, said circuitry comprising:

(a) means for setting a gate voltage of memory cells from a first selected bit line that exhibits leakage current above a threshold value to an initial voltage level;

(b) means for applying a series of overerase correction pulses to said first selected bit line during a selected time period;

(c) means for detecting during said selected time period whether said bit line exhibits leakage current above said threshold value;

(d) means for, if said bit line exhibits leakage current above said threshold value after said selected time period, increasing said gate voltage and repeating the functions of means (b) and (c); and

(e) means for, if it is detected that said bit line does not exhibit leakage current above said threshold value during said selected time period, selecting a second bit line and repeating the functions of means (a) through (d).

9. The device of claim 8, wherein said selected time period is between about 20-100 milliseconds.

10. The device of claim 8, wherein each overerase correction pulse from said series of overerased correction pulses is applied for between about 0.5-2.0 milliseconds.

11. The device of claim 8, wherein means (c) comprises means for detecting after each overerase correction pulse whether said bit line exhibits leakage current above said threshold value.

12. The device of claim 8, further comprising means for setting an error flag if said gate voltage has reached a maximum gate voltage value.

13. The device of claim 8, wherein said initial voltage level is a negative voltage.

14. The device of claim 13, wherein said initial voltage level is approximately -2.0 V and means (d) includes means for positively incrementing said gate voltage in increments of about 0.5 V.

15. The device of claim 13, further comprising means for positively incrementing said gate voltage to a maximum gate voltage.

16. The device of claim 15, wherein said incrementing means comprises:

a comparator, said comparator having:

a first voltage input coupled to a tunable resistance circuit, said tunable resistance circuit configurable responsive to a word line voltage control signal; and

a second voltage input coupled to a second resistance circuit;

said second resistance circuit coupled to a voltage source for providing said word line voltage,

wherein an output of said comparator regulates an output of said voltage source responsive to a voltage signal at said first voltage input.

17. The device of claim 16, wherein an output of said comparator is coupled to an output of said voltage source through a leakage path.

18. The device of claim 8, wherein said memory array is a flash memory array.

19. A method of overerase correction for memory cells in a flash memory array after the memory cells have been erased, comprising the following steps:

(a) setting a gate voltage of memory cells from a first selected bit line exhibiting leakage current above a threshold value to an initial voltage level, said initial voltage level being a negative voltage;

(b) applying a series of overerase correction pulses to said first selected bit line during a selected time period;

(c) detecting during said selected time period after each overerase correction pulse from said series of correction pulses whether said bit line exhibits leakage current above said threshold value;

(d) if said bit line exhibits leakage current above said threshold value after said selected time period, incrementing said gate voltage to a second voltage level and repeating steps (b) and (c); and

(e) if it is detected that said bit line does not exhibit leakage current above said threshold value during said selected time period, selecting a second bit line and repeating steps (a) through (d).

20. The method of claim 19,

wherein said selected time period is between about 20-100 milliseconds, and

wherein each overerase correction pulse from said series of overerase correction pulses is applied for between about 0.5-2.0 milliseconds.

21. The method of claim 20, wherein said initial voltage level is approximately -2.0 V and step (d) includes the step of positively incrementing said gate voltage in increments of about 0.5 V.

22. The method of claim 21, further comprising the step of detecting whether said gate voltage has reached a maximum gate voltage value.

23. The method of claim 22, wherein said maximum gate voltage is about 1.0V.

24. A semiconductor device comprising a memory array including a plurality of memory cells disposed in a plurality of bit lines, said semiconductor device comprising

circuitry for overerase correction of said memory cells after the memory cells have been erased, said circuitry comprising:

a source of overerase correction pulses to be applied during a selected time period;

an overerase verify circuit, said verify circuit detecting whether a selected bit line exhibits leakage current above a threshold value during said selected time period;

a gate voltage source, said gate voltage source responsive to a control signal representing a gate voltage from a plurality of gate voltages to be applied to said memory cells from said selected bit line during application of said overerase correction pulses; and

a bit line selection circuit, said bit line selection circuit responsive to a control signal indicating if it has been detected during said selected time period if said selected bit line exhibits leakage current above said threshold value.

25. A method of overerase correction for memory cells in a memory array after the memory cells have been erased, comprising the following steps:

(a) setting a gate voltage of memory cells from a first selected bit line including an overerased memory cell to an initial voltage level;

(b) applying a series of overerase correction pulses to said first selected bit line during a selected time period;

(c) detecting during said selected time period whether said bit line includes an overerased memory cell;

(d) if said bit line includes an overerased memory cell after said selected time period, increasing said gate voltage and repeating steps (b) and (c); and

(e) if it is detected that said bit line does not include an overerased memory cell during said selected time period, selecting a second bit line and repeating steps (a) through (d).